Advanced Logic Synthesis for Electronics
A.L.S.E. - http://www.FPGA.fr

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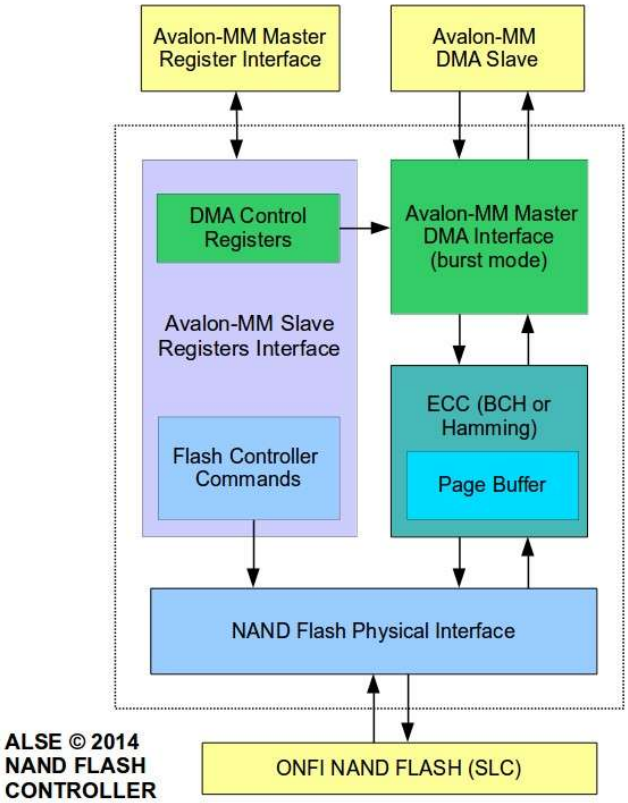
ONFI SLC NAND Flash Controller
Introduction

NAND-Flash memories are attractive due to their high density and low price. However, when compared to Parallel (NOR) Flash Memories, they are challenging because they are not fault-free and they are organized like disk drives, with atomic transfers being a whole “page” (no random read/write with data integrity). As a consequence, they cannot be used as straight replacement: they require a specific Controller.

At A.L.S.E, we have applied our very strong experience in Memory Controllers to take into account this growing demand and we have developed an extremely compact and efficient yet low-cost ONFI SLC NAND-Flash Memory Controller.
A specific version of this controller is optimized in size and performance for Altera devices and Qsys-based systems (with or without embedded processor).

Despite the compactness, the transfer performance achieved is extremely high (embedded DMA engine) while remaining quite simple to use.



The **Main Features** are:

- **High-Performance** Controller supporting 32 bits **DMA Burst** Mode transfers for optimized transfer speed and minimal switch fabric overhead. Use of NAND Asynchronous **Timing Mode from 0 to 5 (fastest)**.
- Supports **2KB, 4KB or 8KB page size**, and latest (at the time of writing this document) NAND memory densities : 32Gbits, 64Gbits, 128Gbits, etc …
  Supports 4 or 5 bytes NAND Address Command**. Supports multiple Dies (CE#) Flash**
- **Avalon-MM** (Memory-Mapped) 32 bits **Slave Interface**. Typically, the Controller will serve a Master that can be an Altera Nios II CPU (32bits), another embedded CPU, or no CPU at all (processor-less applications).
- **Bi-directional Embedded DMA Engine** with Avalon MM Master 32 bits R/W port with Burst Mode support and **Interrupt** generation to minimize CPU overhead.
- Can be integrated seamlessly using **Qsys,** or manually. It is maintained up-to-date with the latest version of the Altera tools (older versions on request).
- **Automatic & Transparent Error Check and Correct** (ECC based on **BCH**, 8bits correction for 512 bytes of Data). Please contact ALSE for more advanced ECC schemes.
  Simpler ECC Hamming code (1bit correction for 512 bytes of Data) is also available.
- **Versatile**. This IP can be used in all FPGA Altera devices (internal memory blocks must be available).
- **Compact**. With ECC BCH enabled (8bits correction), the area is typically around 4,000 Logic Elements, and 10 to 20 memory blocks (M9K) are used (depending the NAND Page Size).
  With ECC Hamming (1bit correction) enabled, the area is typically less than 1,500 Logic Elements, and 4 to 10 memory blocks (M9K) are used (depending the NAND Page Size).
- Provided with Sophisticated **SDC Timing Constraints**, **Reference Design** , example **API**, etc...
  ALSE can optionally test the controller on your custom FPGA board before delivering the IP.
- First-class **Technical Support** (E-mail and Telephone, extended CET hours).
- Very **affordable**. Different license schemes are available. No (zero) Royalty.