Advanced Logic Synthesis for Electronics
The ASIC-FPGA Design Experts

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Quad-SPI Flash Memory Controller

Introduction

Quad-SPI Flash memories initially appeared for BIOS in PC motherboards. The high volumes involved drove prices down, rendering them popular for many other price sensitive applications (e.g. automotive/consumer applications). These Quad SPI Flash memories are available in high speed, low pin count small packages, and they are low cost.

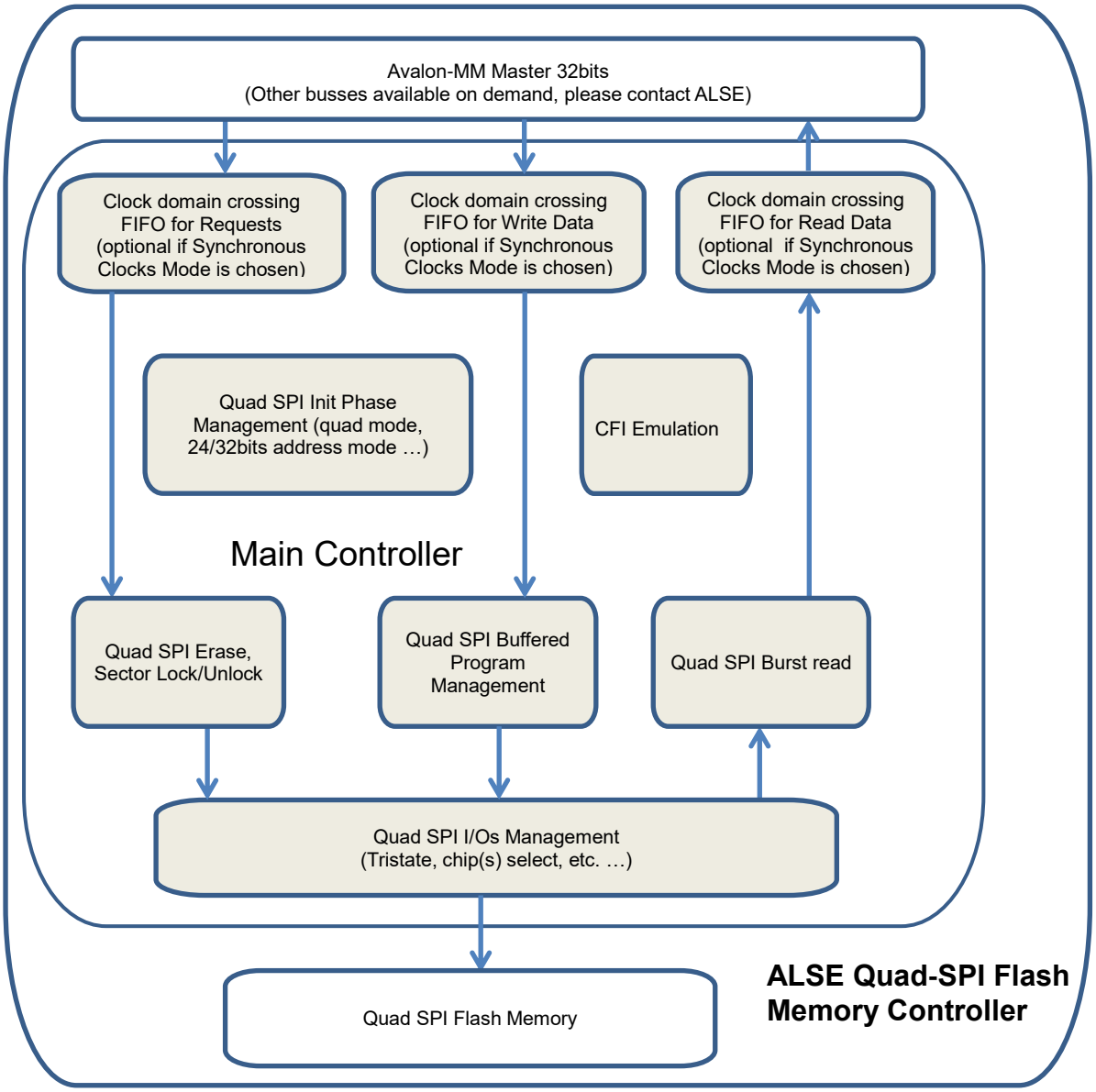
ALSE is addressing this growing demand, by proposing a Quad-SPI Flash Device Controller IP designed for **easy integration into an FPGA**. In order to fit in many different FPGA types, it has been designed for occupy a **very small foot print** while offering **extremely high performance and reliability**.

This efficiency will help you dramatically **reduce your boot time** (for example) and will allow you to use Serial Flash memories with the same performance as parallel NOR Flash memories (bulky, pin & space consuming, more expensive).

Our IP can control all types of Quad SPI Flash Memories (like Spansion S25FL129P, Winbond W25Q80, W25Q16, W25Q32, Micron M25Q256, Numonyx N25Q256, N25Q512, SST26VF016, Macronix 25L256 etc…), including the most recent with capacities larger than 128Mbits (256Mbits, 512Mbits, 1Gbits, etc … Stacked Dies Devices are supported)

If you have a specific Flash device in mind, you can contact ALSE and verify it is supported.

Deliveries include **a HDL simulation environment** for seamless integration in customer project.



Features

- High Performance controller using Burst Mode and multi-lanes (x4) capability for optimized transfer speed (up to ~54Mbytes/s).
- Intelligent aggregation of atomic transfers (bytes, word etc) providing high performance in all situations.
- Synchronous Management of the Quad SPI interface (up to 108MHz, depending on FPGA speed grade and customer-specific Board Timing constraints).
- Can control Quad SPI Flash devices of any size, up to the largest existing size (devices up to 1GB are supported).
- Avalon MM (Memory-Mapped) Slave Interface. Ready-to-use for easy integration in Qsys (hw. tcl), but can also be used in stand-alone mode, without any processor required.
  Other bus formats are available on demand.
- Clock Domain Crossing included for seamless integration. This mode can be disabled if using a full synchronous system, to reduce memory access latency.
- Direct Command Mode available to manage QSPI low-levels commands (lock/unlock, read status, write status, etc …) from the Avalon User Interface.
- Transparent CFI Flash Emulation (optimized for use with Altera Nios-II Flash Programmer). This option greatly facilitates the adoption of the Quad-SPI as a replacement of standard CFI Parallel Flash Memories.
- Modular: Flash programming and many other options (FIFO size, FIFO depth, etc …) can be enabled or disabled at compilation time.
- Complete SDC Timing Constraints provided; Hardware Tester and Software Reference Design (Qsys + nios2)

Speed and Area optimized Quad-SPI Controller for Integration into a FPGA:

- **Compact** (see Implementation results Table, here after)
- **Fast**: on Altera EP3C25F256C6 Cyclone III devices Quad-SPI controller can run faster than 175 MHz
- **Versatile**: can be used on any FPGA device (internal memory blocks are required for the FIFOs)

Implementation Results & Performance

Implementation results using Quartus 14.1 (with Flash Programming Feature Enabled, Synchronous Mode Enabled, FIFO Write Requests in Logic)

* Disabling Flash Programming would remove around 400 LEs / 250 ALMs
* Different schemes are possible for internal FIFOs (in LEs instead of Memory Blocks) for seamless integration.

FPGA Device	Area	Memory Blocks	Multipliers	Max Frequency
Altera Cyclone III / Cyclone IV - Speed Grade C6	~1100 LE's	1 M9Ks	0	~175 MHz
Altera Cyclone V - Speed Grade C6	~500 ALM's	1 M10Ks	0	~190 MHz
Altera Stratix V - Speed Grade C2	~500 ALM's	1 M20Ks	0	~230 MHz

Contact ALSE for implementation results on any other FPGA device family.
More details of implementation results are provided in the complete IP User Guide.

Deliverables and Licensing Schemes

Deliveries can be: Source RTL, Encrypted RTL, or Netlist, depending on licensing scheme selected.

HDL Simulation Environment

- Pre-compiled simulations libraries
- Testbench and Simulation script for ModelSim

Complete User's Guide

Hardware / Software Reference Design

Various licensing schemes

- Encrypted RTL
  - Timed or Untimed
  - Node Locked or floating
  - Single or Multi-projects
- RTL
- Netlist (per project or for multiple projects)