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Advanced Logic Synthesis for Electronics
www.ALSE-FR.com

ALSE UART Tutorial for the Igloo nano Kit

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- **Digital Design** course
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Copyright Notice

Introduction

This Application Note describes how to get and install the Actel tools, the Igloo nano Board, and how to implement and test a small FPGA VHDL project on the **Igloo nano Kit**, using Actel Libero.

This project includes a simple version of the ALSE **UART**, to be used in this Tutorial only.

All the source files are provided ready to be used and you do not have to code anything.

The steps to install the tools and the hardware, to build the FPGA project, synthesize, Place and Route, program the Igloo device, and run the tests on the board are all detailed here.
This entire Tutorial can be performed in less than one hour.

Pre-requisite

You must have a PC under Windows (XP) with **Libero Gold 8.5 (free)** properly installed and licensed. We detail all this installation in this Tutorial.

You must have an Igloo nano Kit (< 50 US $). This Kit can be purchased for example at :
http://www.mouser.com/Search/Refine.aspx?Keyword=AGLN-Z-NANO-KIT

So, with a PC and for less than 50 $, you can follow this Tutorial completely.

Read this document if you want an introduction to RS232 and UARTs.

Beware: Rights of use

Beware that the UART provided here by ALSE is **not free** !

If you want to use it in any real project for any other purpose than education, you must purchase the license at ALSE.

Installing the Tutorial Files

If you received an auto-extractible archive, just run it and select C:\ as the installation directory.

Otherwise, create the sub-directory structure and copy these files :

`C:\ALSE`	Use this location.
`C:\ALSE\Igloo_nano`	Igloo nano Kit demo sub-directory, contains this document.
`C:\ALSE\Igloo_nano\Src`	copy here : **uart2400.vhd**, **applic.vhd**, **top_uart.vhd**

Also : make sure the Igloo nano Kit & Flashpro drivers are installed, and verify that jumpers are seated on JP13-14-15. All this is explained in details in the next pages.

Installing Actel Libero IDE

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Prerequisite

The computer on which Actel Libero will run must have the following characteristics :
powerful PC with Pentium processor or compatible, Windows XP (or Vista), at least 512 Mb of Ram (XP) and preferably 1G Ram or more, approximately 3 GBytes of free Hard Disk space, display: 1024 X 768 or higher, DVD-ROM (if Libero installed from a DVD).

*Beware: you must have **administration rights** on the computer to install the software, the license (environment variable) and the USB drivers.*

A valid Libero Gold license is necessary for this Tutorial. For a lot of Actel devices, the free « Gold » version is sufficient and can be obtained (for free and very quickly) by contacting Actel on the Web (see below). This free license is valid for 12 months and can be renewed.
Important : the « Evaluation » license does NOT allow the generation of programming files (*bitstreams*) and, by consequence, will *not* be suitable for this Tutorial.

☞ For this Tutorial, you must install, license and use *Libero Gold Free version 8.5*.

Obtaining the Libero Software

During our Training courses, you may use the DVD that ALSE has created specifically.
For this tutorial, you might be able to use the DVD that came with the Kit **if version 8.5**, but it is also possible to download the latest version directly from the Actel Web site :
http://www.actel.com/download/software/libero/default.aspx.
To date, Libero is version 8.5 SP1 (as of March 2009). Be prepared to download a couple Gigabytes...
For this Tutorial, you can use either version 8.5 or 8.5 SP1.

Note that there is also a version of Libero suitable for Linux.

Obtaining a License

To use Libero, you need a valid license. To obtain a **free one-year Libero Gold license** :

- Go to : **http://register.actel.com/RegSerial.asp** and select « **Free license**» .
- Select : **« Libero Gold Node Locked for Windows »** for the free version.
- Select the Operating System (this selection has no consequence).
- Enter your Disk Id (use the "**vol c:**" command for example).
- Submit your request. You should receive quickly the license by e-mail.

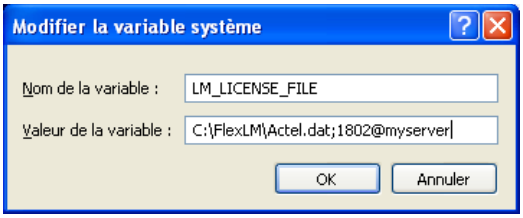
Note : during the process above, you may be asked to create an account. Proceed as suggested until you have a valid Actel account which is necessary to receive the license. Carefully remember your account information for later use.

Beware : As previously mentioned, an « Evaluation » license does NOT permit the generation of programming files, thus preventing you from using the Actel Board during the Tutorial ! Make sure you install a **free Gold license** which also covers ModelSim-OEM (not used in this Tutorial).

Installing the License

The E-Mail you receive from Actel (with the license) also contains information about how to proceed.

- Create a directory named **C: \ FlexLM**
- Save the license as **C: \ FlexLM \ Actel.dat**
- Add **C: \ FlexLM \ Actel.dat** in your **LM_LICENSE_FILE** Environment Variable.
  (Windows key / Pause, Advanced tab, Environment Variables, System Variables)
  NB : you can add this path to an existing contents by pre-pending it and using a semi-column as separator : add « **C: \ FlexLM \ Actel.dat;** » *in front* of the current variable's contents.



NB : we have added spaces for readability, do not use spaces in the actual paths !

Installing Libero

MAKE SURE you are installing the Version that matches your Operating System !

- If you received a DVD from ALSE, run **setup.exe** located in the "**\Libero**" subdirectory.
  The 8.5 version on the ALSE DVD is for Windows XP/Vista.
  Note: if you quickly see an error window with no meaningful message, just acknowledge it: the installation may continue and be successful.
- If you downloaded from Internet, run **LiberoIDE85.exe**, (as of Feb 2009), select a **temporary location** on your hard disk with lots of room available -more than 2GB is currently required-) that will be used for uncompressing the installation files ! The installation itself then will consume an*other* ~3 GigaBytes. These uncompressed installation files will *not* necessarily be cleaned up automatically after the installation, in which case you should **remove them manually** at the end of the installation. This explains why you may need **more than 3 Gb** or free hard disk space during the installation.
- License type : select ***Libero Gold.***
- Accept the copyright panels and confirm the **installation path** where you want Libero to reside in.
  It is strongly recommended to **accept the proposed path**. Changing the drive is fine.
  It is absolutely necessary to **avoid paths that include special characters or spaces**.
- Select among the list of supported devices and families. If you want to optimize the disk space, you can keep only some device families (keep at least the Igloos for this Tutorial !).
  Confirm and be patient while the installation process runs (this may take a while, especially if an anti-virus program is active). You will see some other tools being installed automatically.
  You will probably have to restart the computer when the installation is complete.
- At this point, you may install the latest **Libero Service Pack**, if applicable to your version.
  As of March 2009, the Service Pack 1 for v8.5 is available.

The installation of Libero is now complete.

- **Launch Libero**, for example with : Start ► Programs ► **Actel Libero IDE 8.5 ► Project Manager**
  Alternatively, you can use the **Libero icon on the desktop**.
  If the license is not correctly installed and valid, the software will complain.
- If all seems correct, you should now **erase** the temporary installation files that may have been left.
  If you installed from the DVD provided by ALSE, this step may not be necessary.

Installing & Setting up the Actel Igloo nano Kit

You must have already installed and licensed the Libero 8.5 Gold software, and you must have an active Internet connection or the CP2102 driver.

Igloo nano Board

- Unpack carefully the **Igloo nano Board**.
- Install the four spacers and screws. If necessary, remove the protective sticker on the DIP Switches.
- Install **20 jumpers** (total) on **JP14, JP13 and JP15**.
- **Connect** the Actel Igloo nano Board to the PC using one of the provided **USB** cables.
- Windows should detect a **New USB device** : "CP210x USB to UART Bridge"
  If it does ask you to install the driver :
  - If you have an active Internet connection, you can try an automatic installation.
  - If this above fails, you can install the driver manually using the driver archive that you can download from https://www.silabs.com/products/interface/usbtouart/Pages/default.aspx

Low Cost Programming Stick

- Unpack the LCPS programming stick. Do not plug it into the Igloo nano board yet.
- Connect the LCPS to your PC with one of the provided USB cables.
  Windows should discover a new USB Peripheral.
- Select "Not this time...", then "Install manually from a list...", then select the proper installation path for the FlashPro drivers which could be for example :
  C:\Actel\Libero_v8.5\FlashPro\Drivers\auto
  Windows should install the driver (you may have to **confirm**).
- Normally, Windows will discover *again* a new device ! This is normal...
  Proceed again exactly as above (manual install, same location for the drivers).

Connecting the Programmer and the FPGA Board

- Un-connect the Igloo nano Board and the LCPS from the PC.
- Attach the LCPS to the Igloo nano Board **matching pins 1**.
  The LCPS should have the 24 MHz Quartz (and the USB plug) up on the visible side.
- Connect again the Board and the LCPS to the PC.

You're set !

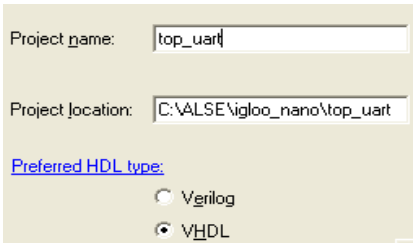
Implementing the ALSE UART Project with Libero

Creating the Project

- Launch **Libero** : **Start** Menu ► **Programs** ► **Actel Libero IDE 8.5** ► **Project Manager**
  or use the icon on the Desktop (if installed).

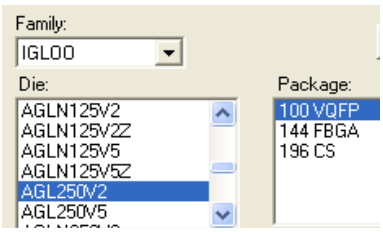
- **Project** ► **New Project**.
  Project location = **C:\ALSE\Igloo_nano** :
  Project name = **top_uart**

  Select (activate) the **VHDL** box
  click **Next >**



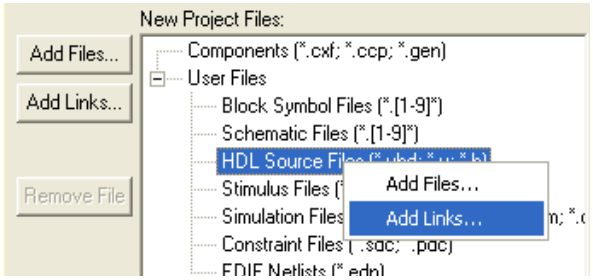
- Select the proper **Actel Device** :
  Igloo AGL250V2 - 100VQFP

  Click **Next >** twice.

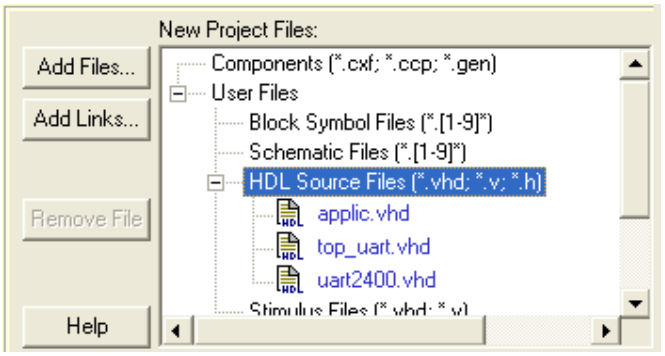


From the last window, we will **add links** to the design VHDL files.

- Right click on **HDL Source Files** , select **Add Links**.



- Browse to c:\ALSE\Igloo_nano\Src and select :
  uart2400.vhd, **applic.vhd**, and **top_uart.vhd**
  then **Add**.

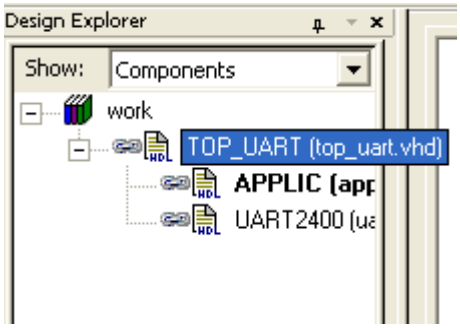


Important In general, you should **avoid using** the **Add Files** option :
this option creates a copy of the original source files under top_uart**hdl** **!**
If you modify an original *file, Libero will NOT see the change.*
If you modify a copy*, the* original *won't be updated.*
Since Libero Version 8, we can **Create a Link** towards an original file instead, which is usually a better option.

- **Finish** : the project is now created.

At this stage, we may need to tell Libero that our **top level** is top_uart :

- In the Design Explorer window, **Right-click** on **TOP_UART**, and **Set as Root**.
  The root (top level of the design) is displayed in **bold** characters.



- **Project > Save project.**

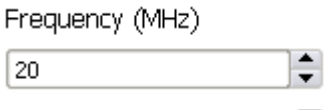
Logic Synthesis with *Synplify*

We are now going to use the OEM (Actel) version of Synplify (from Synplicity / Synopsys).

- From within the « Design Flow » view, click on :

  This opens the Synplify Graphical User Interface.

- Enter **20** MHz in the **Frequency** box (which may not be visible, being located on the far right side)



- Click on the (big !) **RUN** button.

- The synthesis must occur without error (the four warnings are normal).
  The proper netlist is created for Actel Designer and you will see some post-processing that creates the post-synthesis model.
  The usual FPGA design flow doesn't really require to perform post-synthesis pre-layout simulation.

- **Close *Synplify*** (you can save -or not- the Synplify project).

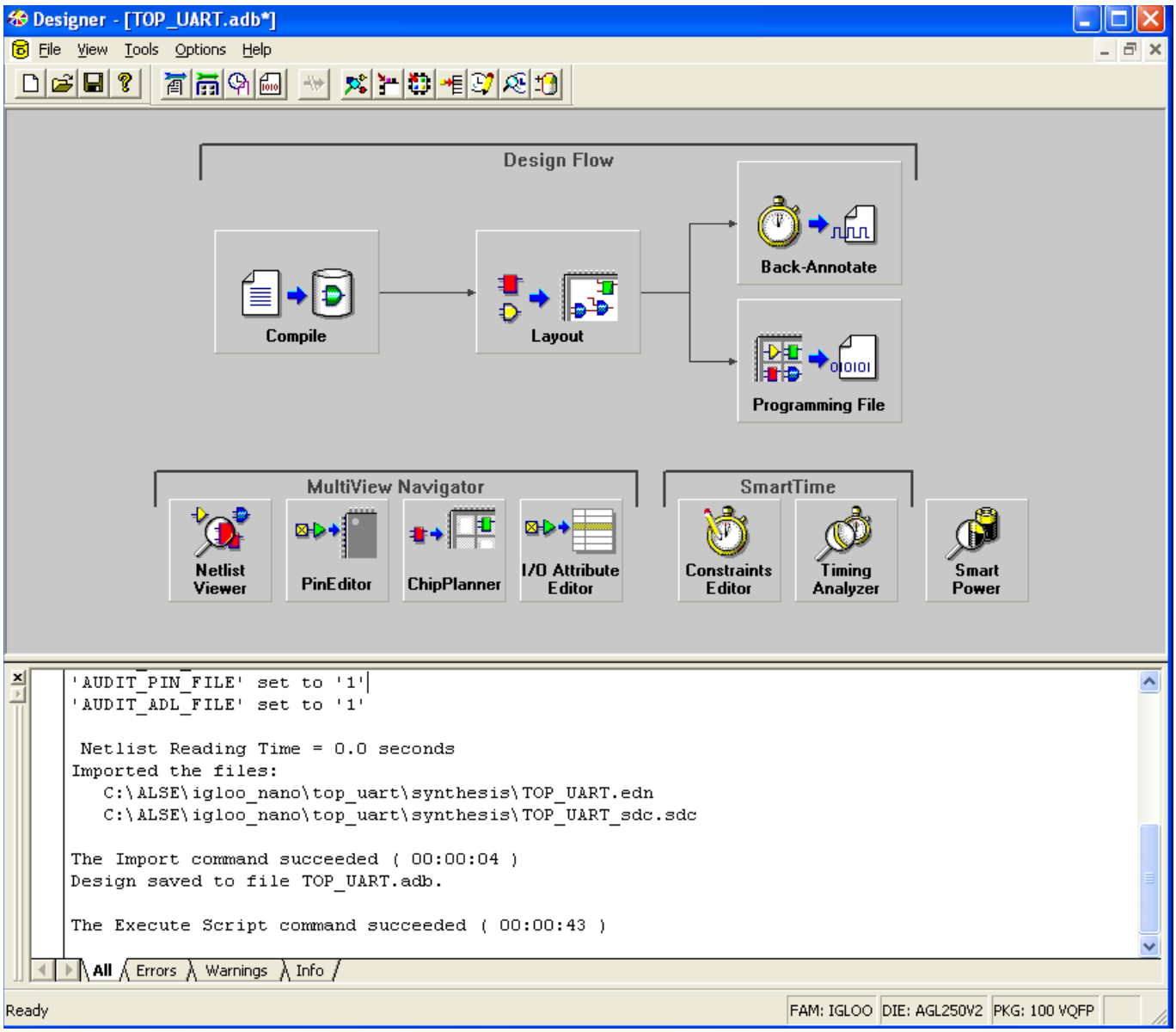
Place & Route with *Actel Designer*

This step will start from the *netlist* generated by Synplify to Map, Place and Route the logic in the FPGA. It is often referred to as "*Layout*", "*Place & Route*" or also "*Fitting*".

- Click on : 

- You must **select** the exact device used on the hardware platform : type, reference, package, supply, speed grade, default I/O format etc... If needed, check with the board you are using.
  For the **Igloo nano Kit** : **AGL250V2-100 VQFP, STD 1.2V, I/O LVCMOS 3.3V, Range COM**.

  This brings the following pane :



The next step is to let Actel Designer analyze ("**compile**") the design in order to discover and check the contents (from the *netlist* file).

- Click on the **Compile** button.
  On the next pane, click on OK to accept the default compilation settings. The compilation should succeed and the Compile button turns Green.

We are now going to **Assign the Pins**.
The table on the right sums up all the assignments to perform.

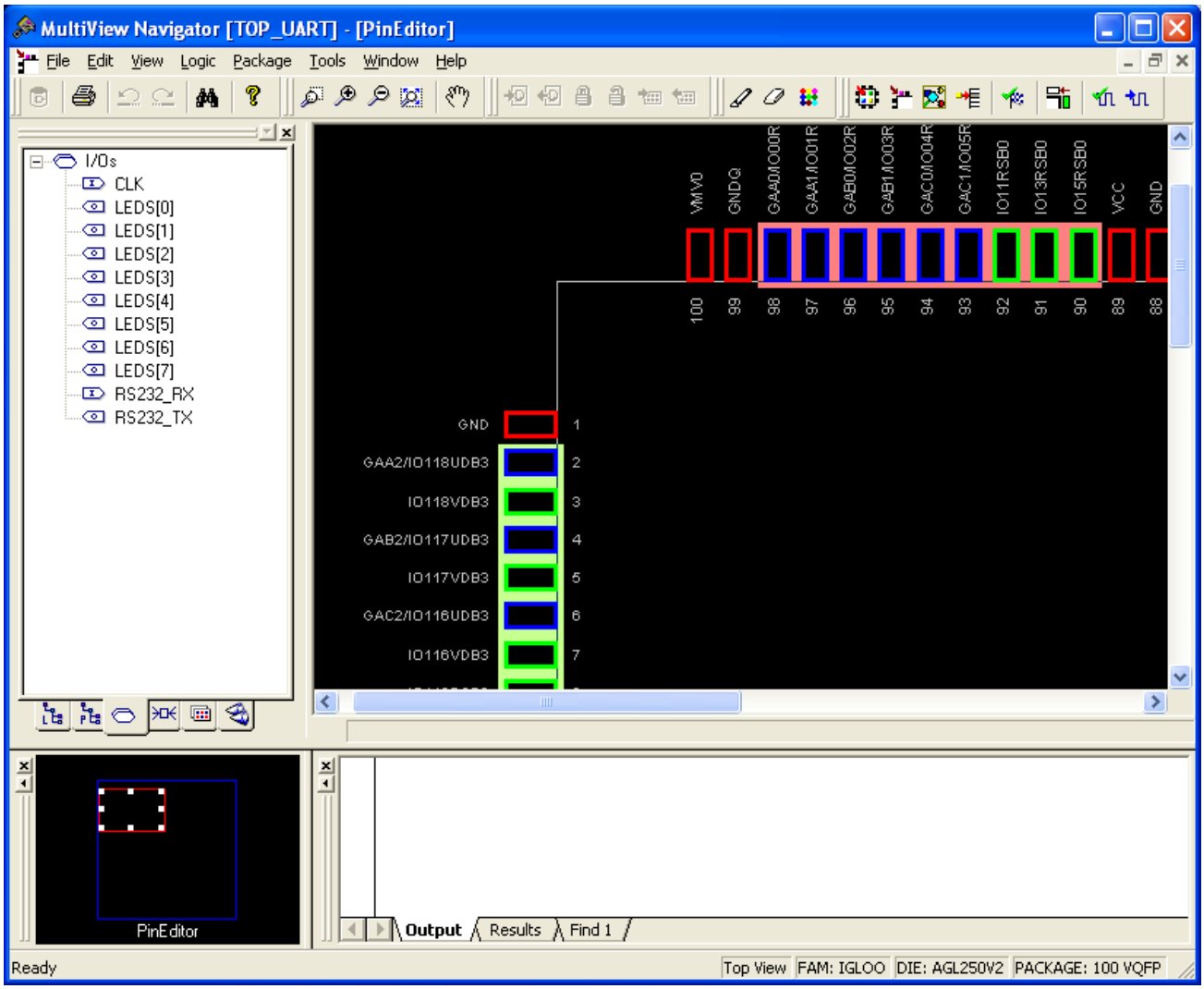
Note that the **DIP Switches** pins (not used in this project) are :
26 - 28 - 29 - 30 - 31 - 32 - 33 - 34

Push buttons pins are : **20 – 21 – 22 - 23**

Pin Name	Location
Clk	15
RS232_RX	16
RS232_TX	19
LEDS(0)	35
LEDS(1)	36
LEDS(2)	40
LEDS(3)	41
LEDS(4)	42
LEDS(5)	43
LEDS(6)	34
LEDS(7)	45

- Click on **Pin Editor**.

- This should to bring up this view :



Use zooming and scrolling commands to display the desired pins.

- Do not forget to activate **this tab** :  in order to restrict the display to I/Os only.

- Using the mouse, **drag** the **Clk** pin from the left window and **drop** it on the desired rectangle in the component view (Igloo nano : **pin 15**).

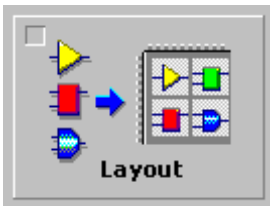
- Use the same method to assign **all** the other I/Os according to the table on the previous page.

- When done, quickly check again the assignment of all the pins.

- When all pins are correctly assigned :
  Click on the **"Commit and Check"** button to record these assignments. 

- **Close** this view.

It's now time to launch the actual implementation **(layout)** of the design for the selected FPGA..

- Under *Designer*, click on : 

and **accept** the default options.

Wait until Layout (Place & Route) has finished (the Layout button turns green too).

Static Timing Analysis

It is important to display and check the **Static Timing Analysis** results.
This will give us the true *Fmax* reached after Place & Route (aka *Layout*).

- Click on the button : 

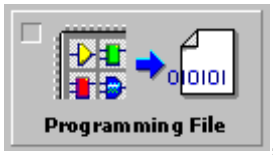
to launch SmartTime.

- Verify that the design will easily work at 20 MHz.

- Click on : **Clk** – **Register to Register** to display the Tsu (slack) histogram.
  You can identify the critical (longest) path (ie *smallest slack*).

- **Close *SmartTime***.

Generating the Programming file

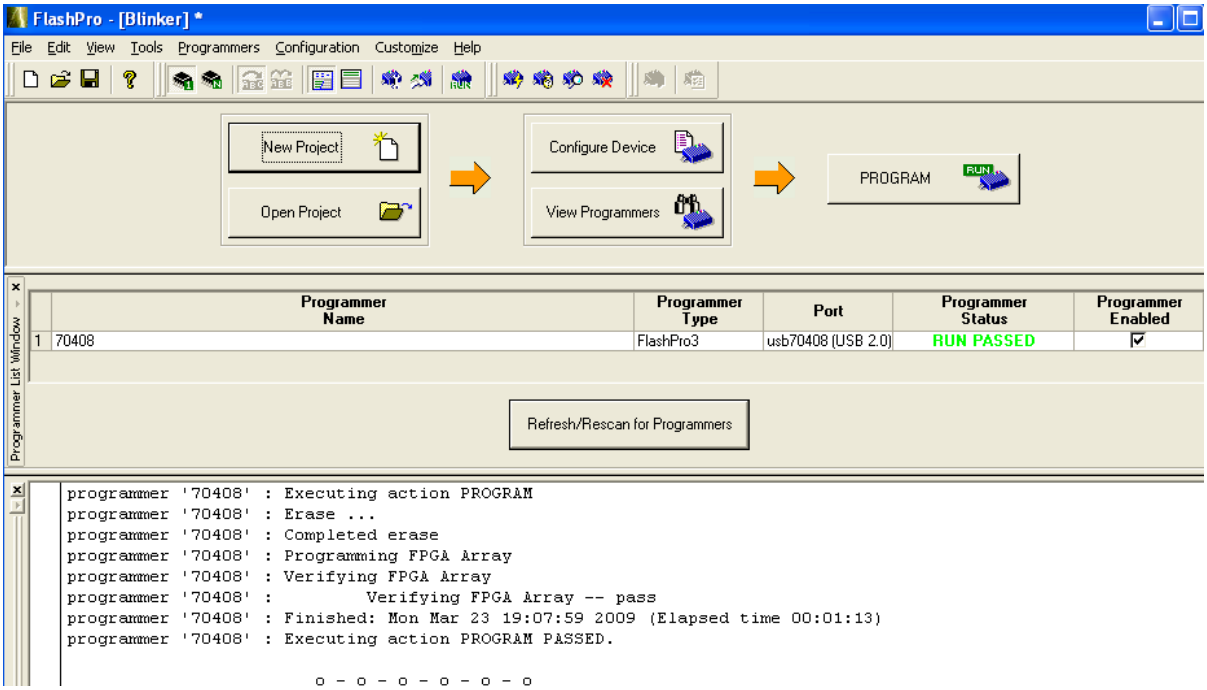
We just have to click on : 

, verify that "**FPGA Array**" is checked, then **Finish**, and **Generate**.
The programming file extension is "**.pdb**" for the **Igloo** devices.

- **Close *Designer*** once the Programming file is generated (save the database when asked to).

Programming the Device

- From within Libero, click on the button labeled **FlashPro**.
- Note that you could create a specific « Flashpro » project, but the default project will do.
- Make sure the LCPS (Programmer device) is plugged in, recognized, and enabled.
  If necessary, click on "Refresh/Rescan for Programmers" until you see the FlashPro3 programmer.



- Click on « **PROGRAM** ».
  Important : the Erase + Program + Verify operations take some time to complete ! This duration depends on several factors, including the device batch, the wear out, etc. For the Igloo nano Kit, the whole process (Erase/Program/Verify) should typically take a bit more than one minute.

If all went well, the LEDs should now display a pattern (Off-On-Off-On-Off-On-Off-On).

- You can **close *FlashPro***.
- You can also **close *Libero IDE*** : our FPGA board is now programmed and ready.

Testing on the Igloo nano Kit

- Open **HyperTerminal**.
  If you don't have HyperTerminal (Vista), download the **free utility : PuTTY.exe** version 0.60 or later.
  http://the.earth.li/~sgtatham/putty/latest/x86/putty.exe
- Select the proper COM port (USB Silicon Labs), which may be COM3 (it may be a different port).
  Select **2400** bauds, **8** data bits, **1** stop bit, **No** Parity, no hardware handshaking protocol (**none**).
- In the Serial Communication Terminal window type a question mark "**?**".
  You should see the ALSE prompt returned by the Igloo board.
- Type in characters, they should be echoed.
- Type the number "1" : a dot "." is echoed.
  Then if you type a string, each character echoed will be offset by 1.
- Type "0" : the offset is removed.

You should also see the LEDs display the ASCII code of the characters that you type.

Note that the ALSE's stand-alone 2400 Bauds UART used in this example project uses only 237 Core Cells (less than 4% of the Igloo device which could then hold 25 such UARTs !). This UART module is provided here under the form of an Igloo netlist but should not be used in another context.
Contact ALSE if you want to purchase one of the source code versions.

Appendix
Useful Pins Assignments

Pin Name	Location
Clk	15
Reset_n	10
RS232_RX	16
RS232_TX	19
LEDS(0)	35
LEDS(1)	36
LEDS(2)	40
LEDS(3)	41
LEDS(4)	42
LEDS(5)	43
LEDS(6)	44
LEDS(7)	45

Pin Name	Location
SW1	20
SW2	21
SW3	22
SW4	23
DIP-SW5(1)	26
DIP-SW5(2)	28
DIP-SW5(3)	29
DIP-SW5(4)	30
DIP-SW5(5)	31
DIP-SW5(6)	32
DIP-SW5(7)	33
DIP-SW5(8)	34

The End

With this small Tutorial, apart from verification (HDL simulation), we've walked through most of the steps in the FPGA Design Flow to implement an HDL Design in an Actel FPGA. You should be able now to start using your own design files and test them in the Igloo nano Kit.

Keep in mind that you do not have any right to use the files provided in your own design, so we do not have to warn you about the legal limitation on suitability etc...

If you have questions, suggestions, ideas,
or if you want to Contact ALSE for any reason,
please fell free to do so :

Bertrand Cuzeau
Chief Technology Officer ALSE
info@alse-fr.com

Please : do not contact us for Technical Support of free demos, free IPs and free Tutorials !
Only paying IPs and customers are entitled to receive our Technical support and Assistance.