

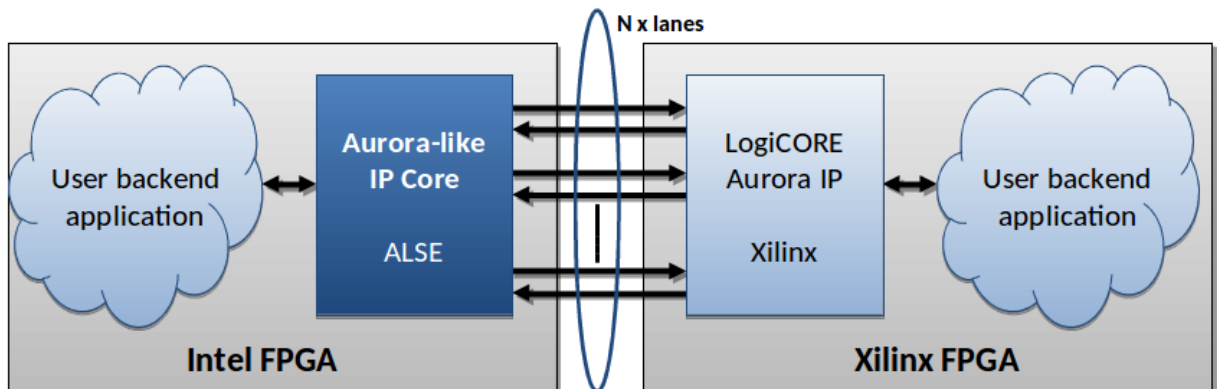
Aurora 8b10b IP Core

Introduction

Aurora 8b/10b is a lightweight protocol suitable for chip-to-chip, board-to-board and backplane communication using high speed transceivers. This ALSE Aurora 8b/10b IP Core targets mainly Intel FPGA devices (formerly Altera), and is compatible with the Xilinx LogiCORE Aurora IP.

This IP core provides an efficient way to interconnect Intel/Altera and Xilinx FPGAs, or any other chip (ASIC, ASSP, etc ...) using the standard Aurora protocol.

Deliverables include a sophisticated HDL simulation environment for seamless development, verification and integration in the final application.



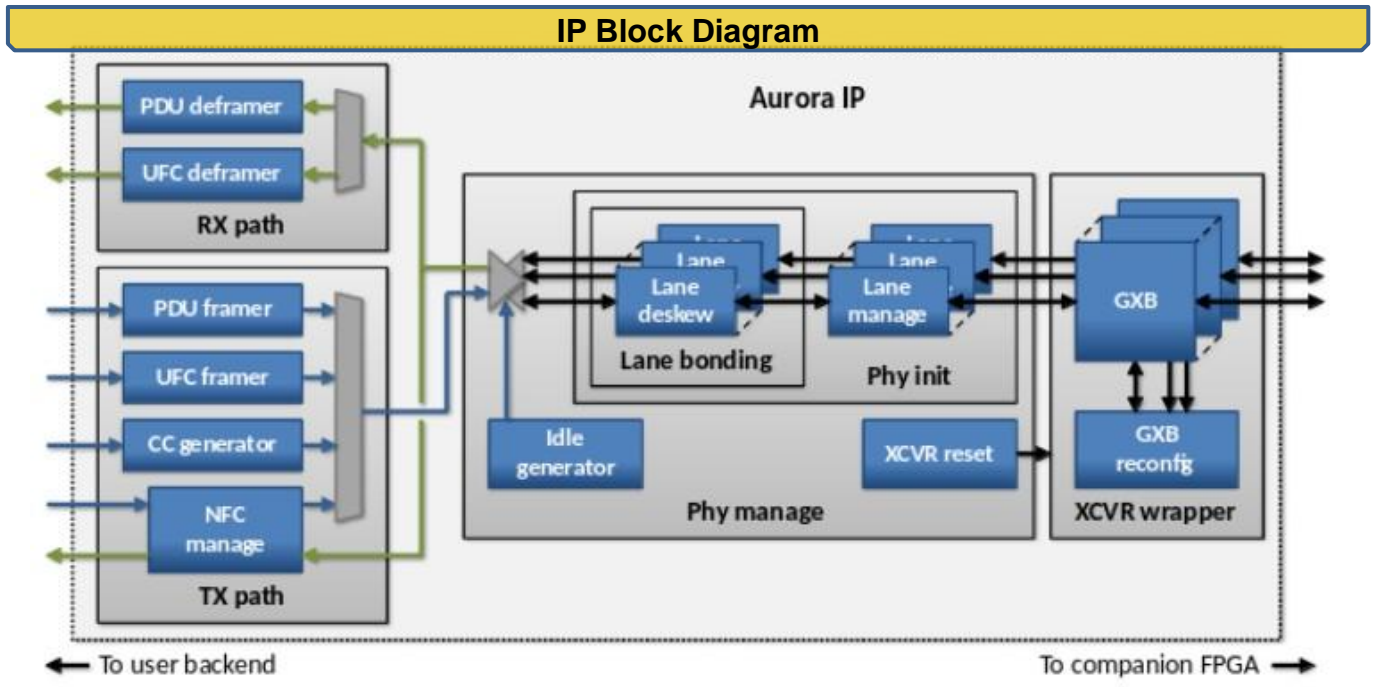
Features

- Fully compatible with the standard Xilinx Aurora protocol
- Up to 16 Transceiver (XCVR) physical lanes
- Link Rate up to Device maximum XCVR Rate with 8b/10b Encoding (e.g Cyclone V GT = 5 Gbps)
- Full duplex and Simplex Tx operations supported
- 8b/10b encoding (please contact ALSE if you are interested by the 64b/66b encoding)
- Framing and Streaming interface
- User Flow Control (UFC)
- Native Flow Control (NFC, immediate/completion modes)
- Additional CRC for PDU Frames
- Clock compensation Sequence Generation
- Per lane polarity inversion, skew compensation
- Avalon-ST / AXI like Streaming user interfaces
- Provided with Hardware Reference designs, QIP files, SDC constraints

Available Reference Designs

- Arria 10 Attila Board <-> Xilinx Virtex7 VC707 : 1 lane @ 6.25Gbps
- Arria 10 Achilles Board <-> Arria 10 Attila Board : 4 lanes @ 6.25Gbps (Intel-FPGAs on both sides)
- Stratix10 GX Dev Kit <-> Arria 10 Achilles Board : 4 lanes @ 6.25Gbps (Intel-FPGAs on both sides)
- Cyclone V Clovis Board <-> Xilinx Virtex6 ML605 : 1 lane @ 3.125Gbps
- Cyclone V Clovis Board <-> Xilinx Virtex7 VC707 : 1 lane @ 3.125Gbps
- etc ...

Please note that ALSE can potentially build a demonstration on any suitable board.



IP Resource Utilization

Intel FPGA Device	XCVR Lanes	Framing / Streaming	Total User Data Path (Data Width per Lane)	ALMs	Memory Blocks (Memory Bits)
Cyclone V	1	Framing	16bits (16bits)	~780	2 M10Ks (4096)
	1	Framing	16bits (16bits)	~930	2 M10Ks (4096)
	1	Streaming	32bits (32bits)	~710	2 M10Ks (4096)
	1	Streaming	32bits (32bits)	~750	2 M10Ks (4096)
	4	Framing	128bits (32bits)	~2930	10 M10Ks (77824)
	4	Streaming	128bits (32bits)	~1750	10 M10Ks (77824)
Stratix V	1	Framing	32bits (32bits)	~1080	4 M10Ks (36864)
	4	Framing	128bits (32bits)	~3100	8 M10Ks (110592)
	4	Streaming	128bits (32bits)	~1950	8 M10Ks (110592)
Arria 10	1	Framing	32bits (32bits)	~520	0 M20Ks (0)
	4	Framing	128bits (32bits)	~2280	4 M20Ks (73728)
	4	Streaming	128bits (32bits)	~1200	4 M20Ks (73728)
Stratix 10	4	Framing	128bits (32bits)	~3000	4 M20Ks (73728)

Note: the numbers above include the transceiver logic.
 Contact ALSE for getting implementation results on any other FPGA device family, or with specific modes (Simplex Tx, CRC).

Deliverables and Licensing Schemes

HDL Simulation Environment

- Pre-compiled simulations libraries
- Testbench and Simulation script for ModelSim

Complete User's Guide

SDC Constraints, QIP integration file

Hardware Tester Reference Design

Various licensing schemes

- Encrypted RTL
 - Timed or Untimed
 - Node Locked or floating
 - Single or Multi-projects
- Source code RTL
- Netlist (per project or for multiple projects)