![A.L.S.E logo] Advanced Logic Synthesis for Electronics
The ASIC-FPGA Design Experts

A.L.S.E's **HPAPB**
Ultra High Performance
Signal Acquisition & Processing
FPGA Board - Stratix V GS Edition

Introduction

This industrial **Signal Acquisition and Processing** board has been designed for acquiring **eight analog channels** synchronously at very high speed (**250 Ms/s**), and implementing very dense and complex signal processing in the biggest and fastest Stratix V FPGA from Altera (now Intel).

With up to **32 Gigabytes** of on-board DDR3 memory (2 slots), **2 x 10G SFP+** slots for 10G Ethernet (eg), and one Gigabit Ethernet port (for control and "low speed" transfers), HPAPB offers unprecedented computing power and communication throughput. An on-board **USB-BlasterII** is included (with extra debug port feature for high data transfer speed).

The external 10 MHz Reference Clock input associated with the PPS input allow extremely accurate (ns) absolute time-stamping, perfect ADC synchronization, as well as multi-boards synchronization.
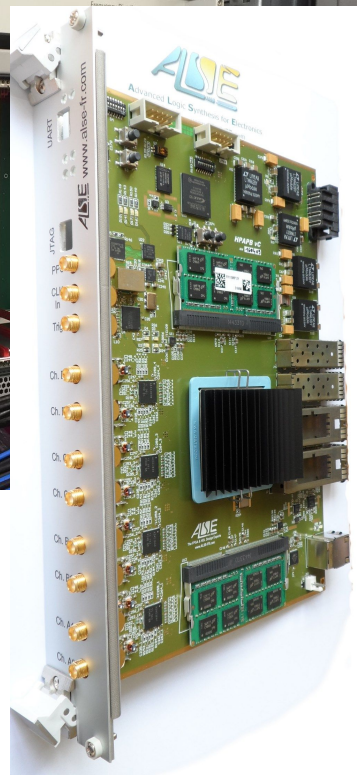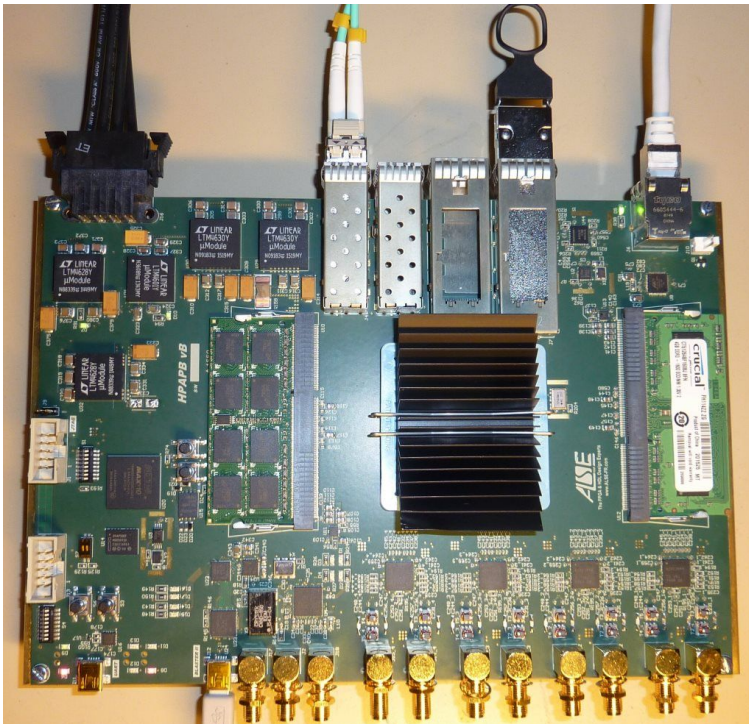
Moreover, it has been designed to communicate at very high speed **(2 x 40 Gbits/s** QSFP+) with neighbor cards (or other equipment), thus allowing cross-computation over an extremely large number of channels (for multiple synthetic aperture, beam-forming, sub-band analysis etc).

For example, HPAPB has been used successfully in a radio-astronomy application with 192 channels acquired and processed simultaneously. An industrial rack, capable of hosting up to 10 x boards, is available upon request (see picture below).
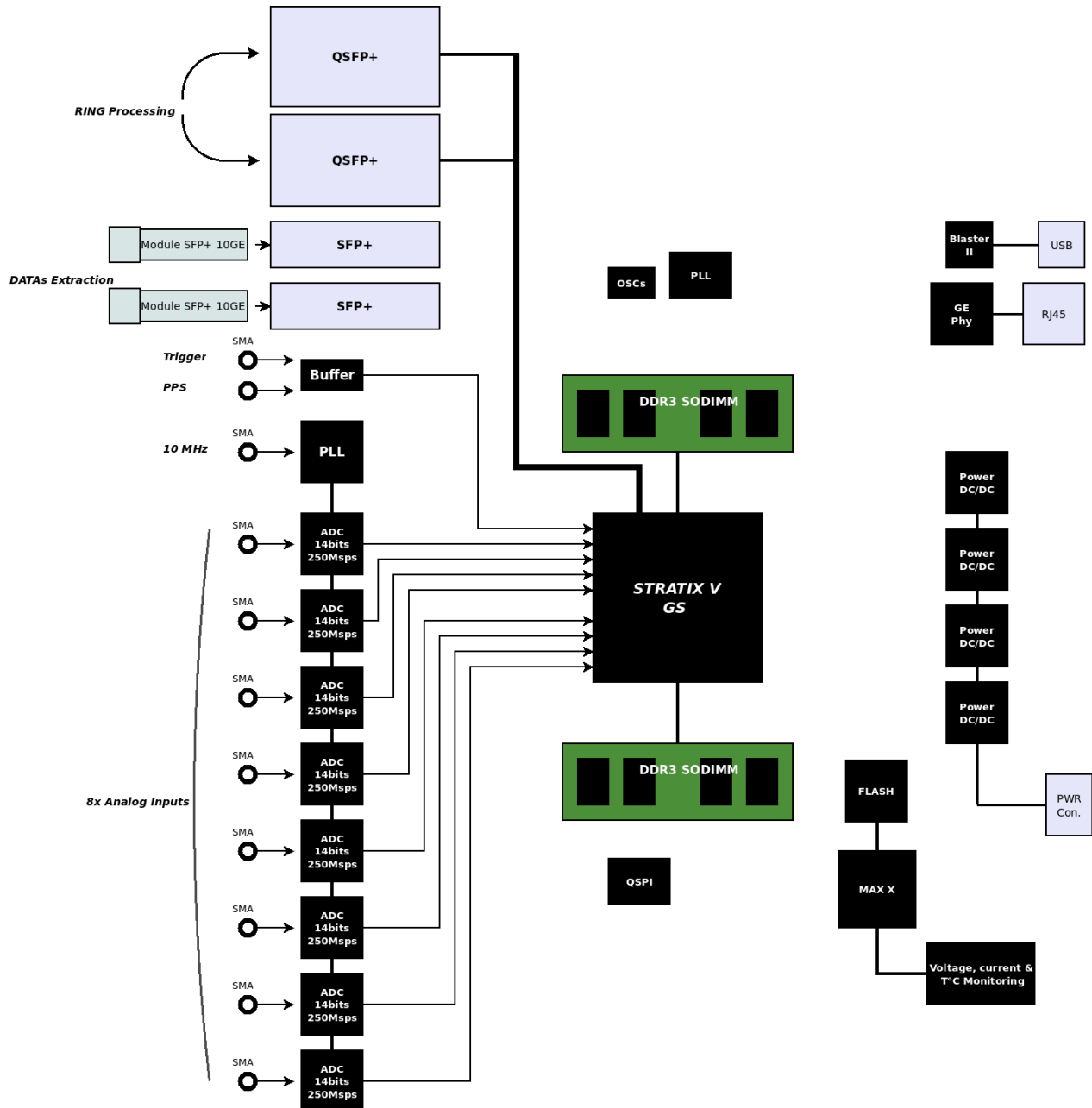
With close to 4,000 internal multipliers, the Stratix V GSD8 FPGA (largest device available) provides huge signal processing power (up to *1000 billions* of multiplications per second !).

With 2 x 40G + 2 x 10G = **over 100 Gigabits** per second for communication throughput, HPAPB can move data between boards or with other processing systems at incredible rates, using standard low-cost cables up to several meters, or optical (fiber) adapters for longer connections.

To help customers take the best advantage of the board's and FPGA's performance, A.L.S.E has developed specific IPs and a very powerful and versatile framework, from ADC data acquisition, to PLLs and synchronization control, to remote firmware update (with management of multiple configurations) through Ethernet, etc.

Block Diagram

RING Processing

QSFP+

QSFP+

Module SFP+ 10GE → SFP+

DATAs Extraction

Module SFP+ 10GE → SFP+

Trigger — SMA → Buffer

PPS — SMA →

10 MHz — SMA → PLL

8x Analog Inputs

SMA → ADC 14bits 250Msps (×8)

STRATIX V GS

DDR3 SODIMM

DDR3 SODIMM

OSCs PLL

QSPI

Blaster II → USB

GE Phy → RJ45

Power DC/DC (×4)

PWR Con.

FLASH

MAX X

Voltage, current & T°C Monitoring

---

250 Ms/s ADCs – 8 Channels

Using Texas Instruments ADS42JB49
 - up to 250Ms/s
 - 14 bits
 - JESD204B serial interface

High perfomance Versatile PLL

Using TI's LMK0482x Ultra Low-Noise JESD204B Compliant Clock Jitter Cleaner with Dual Loop PLLs.
This PLL can be synchronized through the External 10 MHz clock input (like by a Rubidium / GPS oscillator).

Gigabit Ethernet RJ45

A Marvell 88E1310 Gigabit Ethernet PHY with RJ45 is available for (comparatively) low speed communication and board control over Ethernet (110 M bytes/s max).
It is also 100M (Fast Ethernet) compatible.

Versatile Clocks Generation & PLL

A SiLab's SI5338A PLL provides versatile FPGA and SERDES (communication) clocks.

Many on-board high-stability oscillators provide generic or specific clocks.

2 x 10 G (sfp+)

Two SFP+ cages allow using either Direct Attach (passive) cables, Active Copper, or optic fiber modules to implement two 10G Ethernet communication ports (eg).

2 x 40 G (qsfp+)

Two QSFP+ cages allow using either Direct Attach (passive) cables, Active Copper, or optic fiber modules to implement (eg) two 40G communication ports. 40G Ethernet can be implemented, but in many applications, they can be used to link adjacent boards in a "Ring" network that allow sharing data in real time with all other boards in the ring.

High Capacity & Bandwidth Memory

Two **DDR3** SODIMM sockets (running at 800MHz) have been implemented for up to **32 Gigabytes** of on-board memory, to be used by various applications including real time recording, very large buffer, processing memory, etc.

Temperature & Voltage monitoring

The on-die temperature sensor is complemented with external temperature and voltage sensing (3 x dual ADCs) supervised by a Max10 FPGA. This allows implementing safety mechanisms as well as real-time health monitoring applications (and preventive maintenance).

A power fan control with proper connector is implemented that can be driven by PWM with proportional control (eg).

USB – Uart

The mini USB connector with on-board UART chip is a nice touch for system bring-up, monitoring, control, debugging...

High Speed Debugging

The *on-board USB-Blaster II* hardware facilitates the development and debugging phase.
Extra debugging pins (*USB-Debug Master*) provide up to 384 Mbits/s data bandwidth with the PC using the Altera debugging tools (including SystemConsole).

Flexible Configuration

A 1 Gbits **Micron parallel NOR Flash** memory can store several FPGA configuration images (like SAFE + USER). ALSE has developed an IP and Software tools for Remote programming and Flash update through Ethernet.

Another **Micron Quad-SPI NOR Flash** is also available.

Configuration during development and debug can be performed using the **on-board USB-Blaster II**.

Intellectual properties

ALSE has developed a lot of IP blocks (to be purchased separately, if needed) for most board's functions, including:
- JESD204B ADC interface
- High performance 10 G Ethernet communication hardware stack : 10GEDEK,
- Ring inter-board (2x40G) communication

- SGDMA Data extraction for 10G Ethernet streaming.
- High performance Gigabit Ethernet communication hardware stack : GEDEK
- Remote firmware update (Flash) through Ethernet
- etc. Contact ALSE for more details

Custom applications / products

ALSE can also develop very rapidly custom applications using internal know-how and IPs, thus offering a ready-to-use bundle under the form of customized FPGA boards, ready to plug and play.

Reference Designs

The board comes with a "Golden Top" entity and a Reference Design project with all the external devices connected. This is a solid base for deriving easily all kinds of applications, in mere hours.

Typical Applications

- Radio-Astronomy
- Electronic War systems
- Communication and Cable Infrastructure
- Multi-Carrier, Multimode Cellular Receivers
- Radar and Smart Antenna Arrays
- Broadband Wireless
- Test and Measurement Systems
- Software-Defined and Diversity Radios
- Microwave and Dual-Channel I/Q Receivers
- Repeaters
- Power Amplifier Linearization

Your imagination is the limit !

Simple Power Supply

HPAPB is powered through a **single +12V supply**. An 8A (100W) power supply is recommended. The actual input voltage can be comprised between 10V and 14V.

Technical specifications

FPGA: Stratix V GS 5SGSED8N2F46C2N
 - 695k L.Es, 840 I/Os
 - 51Mbits internal ram, 3926 multipliers,
 - 48 x 14.1 Gbits/s transceivers.
Gigabit Ethernet PHY: Marvell 88E1310.
2 x QSFP+
2 x SFP+
Power consumption < 100 W, single +12V supply
Dimensions / form factor: double-europe (233.35 x 160 mm)
PCB: 16 layers, laser vias, Megtron6 material.

Availability and Contact

A.L.S.E
8 passage Barrault
75013 – PARIS – France
tel +33 1 84 16 32 32
info@alse-fr.com
www.FPGA.fr

Advanced Logic Synthesis for Electronics
www.ALSE.fr