Advanced Logic Synthesis for Electronics
The ASIC-FPGA Design Experts

JPEG Decoder

Introduction

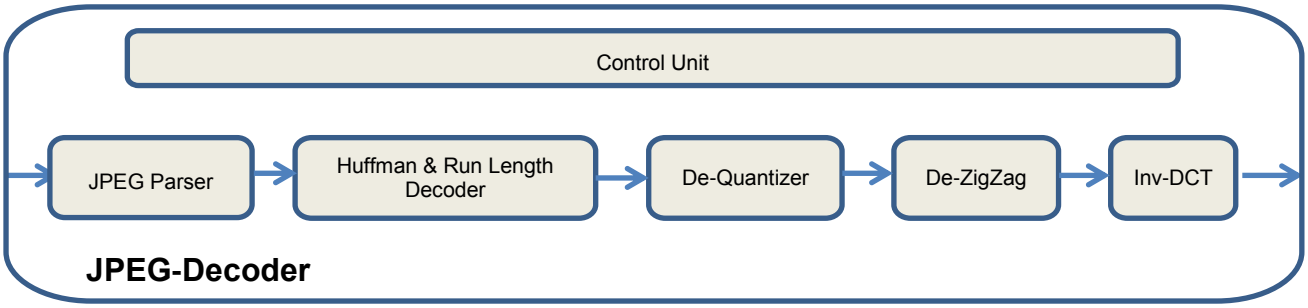
This **JPEG-Decoder IP** has been optimally designed for **easy integration into any FPGA**: the footprint is **very small**, the code is portable to **any vendor**, and the **performance** (Fmax, Throughput, and Image Quality) is high.

It can decode **Still Images and Video Streams**. The JPEG-Decoder comes with **Block to Raster Converter integrated**.

It is a perfect companion for the ALSE JPEG-*Encoder* for creating a complete compressed video transmission chain.

A sophisticated HDL simulation environment is available to facilitate the integration of the IP in the customer project.

Low cost **Demo** platforms for Altera, Lattice and Xilinx are available (contact ALSE for Actel-Microsemi).



Features

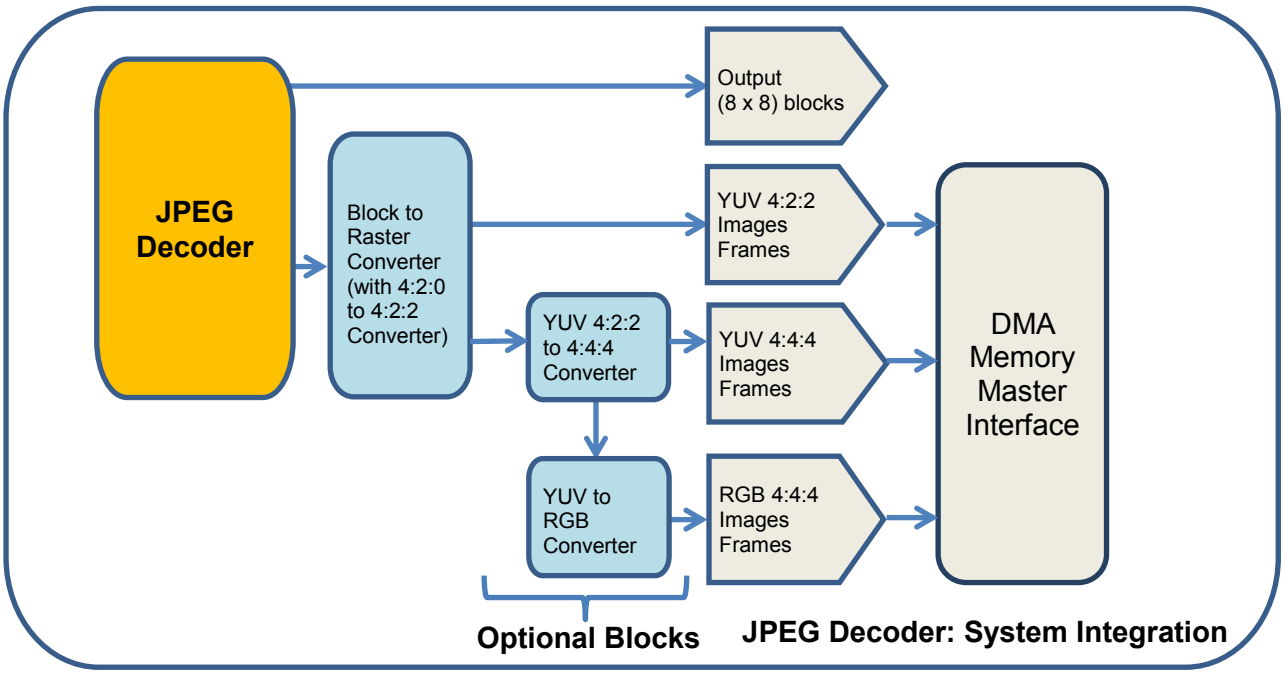
Decoder for Still Images & Real Time Compression

- Baseline JPEG-Decoder
- 8 bits samples
- Supports any image resolution up to 64K x 64K
- Input : Standard JPEG input stream
- Output stream: 8 x 8 YUV blocks (4:4:4, 4:2:2, 4:2:0)
- Standard Huffman Table
- Quantization tables dynamically extracted from JPEG stream

No external Ram required for JPEG Decoder alone

Highly optimized Speed & Area: Ideal for FPGA projects !

- **Compact** (see Implementation results Table here after)
- **Fast**: on Altera EP4CE6E22C6 Cyclone IV device, the JPEG Decoder can run at 180 MHz
- **Versatile**: can be used on virtually any FPGA (internal memory blocks are required).



Easy System Integration:

- Single clock full synchronous design
- Input : simple JPEG 8 bits Stream with backpressure
- Output Video format choice:
  - 4:4:4 / 4:2:2 / 4:2:0 YUV blocks
  - Raster YUV (4:2:2)
  - Raster 24bits RGB (4:4:4)
  - Raster 24bits YUV (4:4:4)

Other possible options:

- DMA with Avalon Memory Master (MM) Interface (SOPC Builder/Qsys compatible) with pixels/lines address generation, and Configurable data width (16bits or 32bits)
- For other system busses, please contact A.L.S.E.
- Frame Buffer Management for Video streaming & Still Images
- VGA, BT656, HDMi, DVI Generators

Implementation Results & Performances

Implementation results on Altera FPGAs (samples) using Quartus 12.1

FPGA Device	Function	Area	Memory	Multipliers	Frequency
Cyclone-III or Cyclone-IV -C6	**Decoder alone**	3700 LE's	5 M9K	9 (18 x 18)	184 MHz
Cyclone-III or Cyclone-IV - C6	Block to Raster (4:2:2 mode)	200 LE's	2 M9K	0 (18 x 18)	>200 MHz
Cyclone-III or Cyclone-IV -C6	Decoder + Raster to Block	3900 LE's	7 M9K	9 (18 x 18)	184 MHz
Cyclone-V -C6	**Decoder alone**	1500 ALM's	5 M10K	9 (18 x 18)	179 MHz

Contact ALSE for implementation results on any other FPGA device family.

Deliverables and Licensing Schemes

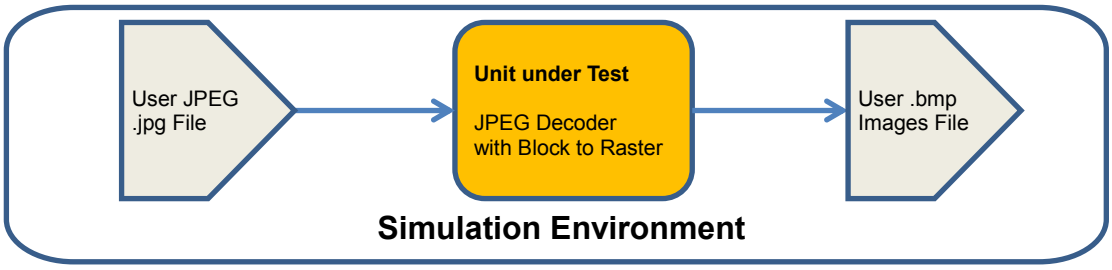
Deliveries can be RTL or Encrypted RTL or Netlist depending on licensing scheme

Sophisticated HDL Simulation Environment (option):

- Pre-compiled Modelsim simulations libraries
- BMP output file generation from JPEG stream input
- Testbenches and Simulation scripts for ModelSim

Various licensing schemes are available:

- Encrypted RTL
  - Timed or Untimed
  - Node Locked or floating
  - Allowing multi-projects generations
- RTL
- Netlist (per project or for multiple project)



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