Advanced Logic Synthesis for Electronics
The ASIC-FPGA Design Experts

JPEG Encoder

Introduction

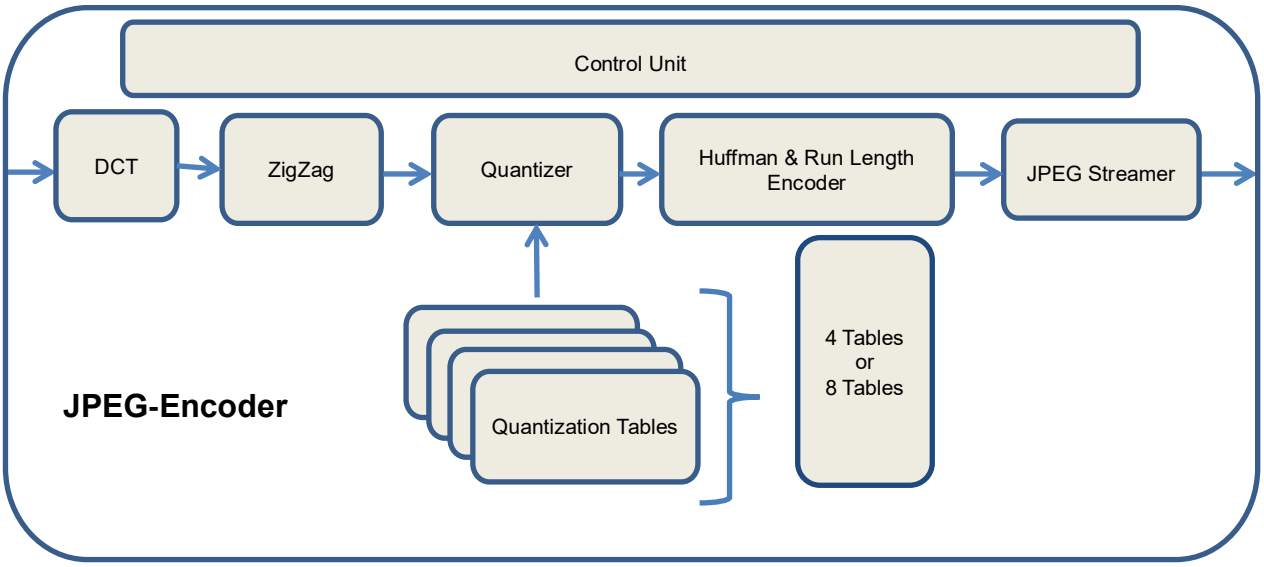
This **JPEG-Encoder IP** has been designed for **easy integration into FPGAs from any vendor**. It has been highly **optimized** for a **very small footprint** and an excellent **Fmax** allowing the use of low cost FPGAs. This IP enables FPGA-based applications to outperform DSP-based solutions and to address the most challenging markets.

The JPEG-Encoder IP can compress **Still Images and Video Streams** and it comes **with Raster-to-Block** conversion integrated.

Several popular input formats are supported natively (BT656, YUV, RGB), thus simplifying the connection to various image sensors or video streaming sources (Video Codecs, Ethernet streams etc).

Deliverables include a very sophisticated HDL simulation environment for seamless development, verification and integration in the final application.

Demos are available for many **Altera**, **Lattice** and **Xilinx** kits (contact ALSE for Actel-Microsemi).



JPEG Encoder Block Diagram

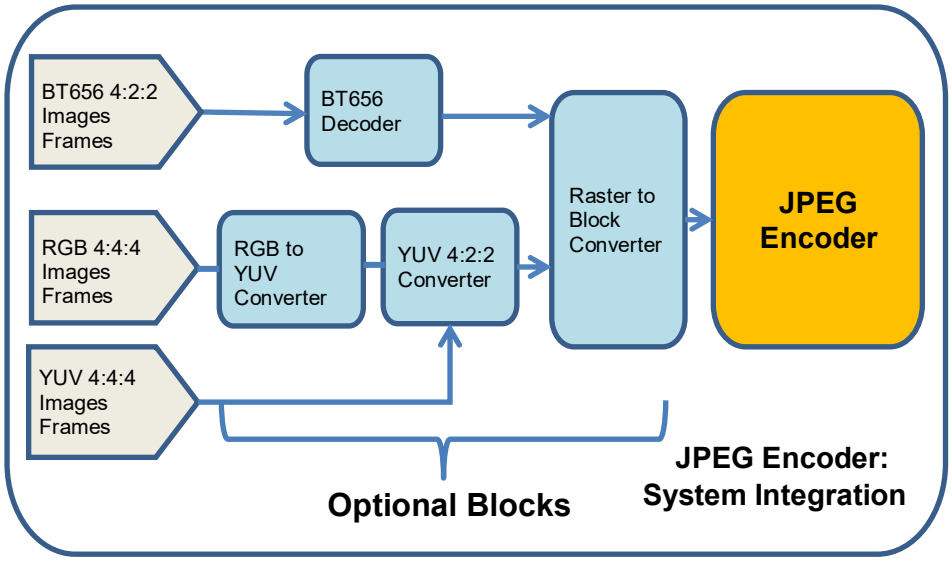
Features

JPEG Encoder for both Still Image and Real Time Video Compression

- Baseline JPEG-Encoder.
- Supports any image resolution up to 64K x 64K images.
- Input stream: YCrCb 4:2:2 (other subsampling schemes can be implemented upon request).
- BT656/RGB/YUV streams handling (see after).
- 8 bits samples.
- Standard Huffman Table.
- Dynamically configurable quantization tables (up to 8 tables) for multiple levels of compression.
- Dynamic choice of compression level.
- 8 Bits (byte) Streaming Output Interface.
- Encoding at approximately 1.16 pixel per clock cycle.
- No external RAM required for JPEG Encoder alone; Raster to Block requirements depend on line size (see note on Table of Implementation results, here after.

Speed and Area optimized

- **Compact:** see implementation results table, here after.
- **Fast**: on Altera EP3C25F256C6 Cyclone III device, the Encoder can run at more than 150 MHz.
- **Versatile**: can be used on all kinds of FPGAs (internal memory blocks are required).



Easy System Integration:

- Single clock, fully synchronous design
- Input Video format choice:
  - ♦ BT656 (4:2:2 YUV format)
  - ♦ 24bits RGB (4:4:4)
  - ♦ 24bits YUV (4:4:4)
  - ♦ Other: contact ALSE
- Output: standard JPEG 8 bits Stream
- Easy connection to A.L.S.E GEDEK (Ethernet Communication Engine IP) for streaming over Ethernet.

Implementation Results & Performances

Examples of Implementation Results: Altera Cyclone families

FPGA Device	Function	Area	Memory	Multipliers	Frequency
Cyclone-IV speedgrade C6	**Encoder alone**	3700 LE's	7 x M9K	4 (18 x 18)	170 MHz
Cyclone-IV speed grade C6	Raster to Block (1024 pixels lines) + BT656	200 LE's	8 x M9K *	4 (18 x 18)	170 MHz
Cyclone-IV speedgrade C6	Encoder + Raster to Block + BT656	3900 LE's	15 x M9K *	4 (18 x 18)	170 MHz
Cyclone-V speedgrade C6	**Encoder alone**	1700 ALM's	15 x M10K	4 (18 x 18)	190 MHz

* In case of 1920 pixels lines, 8 extra memory blocks are required (used in Raster to Block).

Contact ALSE for implementation results on any other FPGA device family.

Deliverables and Licensing Schemes

Sophisticated HDL Simulation Environment

- JPEG stream generation from BMP input file (other formats available upon request, contact ALSE).
- Output capture with JPEG file reconstruction.
- Test benches and Simulation scripts for ModelSim.
- Pre-compiled simulations libraries.
- User's Guide.

Flexible Licensing schemes

- No (zero) royalty.
- Encrypted RTL
  - ♦ Timed or Untimed
  - ♦ Node Locked or Floating
  - ♦ Single or Multi-projects
- RTL.
- Netlist (per project or for multiple project).